IN THE SPECIFICATION:

Please amend the first paragraph in the BACKGROUND OF THE INVENTION section as follows:

> The present invention includes memory and an information apparatus which may be applied, for example, to a read only memory, random access memory, or to an apparatus utilizing these memories. The present invention also includes a memory which may increase its capacity with a simplified process. Moreover, the invention includes an information apparatus utilizing this memory by generating data cell ~~region with the~~ regions using a process other than that used to generate the system region to control data cells.

Please amend the third paragraph in the BACKGROUND OF THE INVENTION section as follows:

> In a conventional semiconductor memory, such as ~~represented by~~ a dynamic random access memory (DRAM)~~, etc.~~, data cells may be formed by a charge accumulation mechanism and are arranged in the shape of a matrix. Access is made to these data cells from a system region. Thereby, data may be written by accumulating charges to the desired data cells corresponding to a cell address. Data is read out by detecting the accumulated charges held in these data cells.

Please amend the second full paragraph on page 2 as follows:

> ~~However, the~~ Creation of conventional semiconductor memory requires large-scale facilities, such as a clean room and stepper~~, etc.~~, for the ultra-fine manufacturing process. Particularly[[,]] when memory capacity is increased by modifying a design rule, ~~such memory capacity is accompanied by a disadvantage in that, to account for modifying a design rule,~~ the facilities for such ultra-fine manufacturing ~~also~~ must be updated or newly constructed, ~~and~~ raising unit price per bit ~~increases, although the integration rate is as much increased~~.

Please amend the first paragraph in the SUMMARY OF THE INVENTION section as follows:

In view of overcoming ~~such disadvantage~~ the disadvantages of the related art, the present invention produces the data cell region and system region with different manufacturing processes.

Please amend the fifth paragraph in the BRIEF DESCRIPTION OF THE DRAWINGS section as follows:

Figs. 5A to 5E are cross-sectional views for explaining generation of word lines of a data cell region of Fig. 1.

Please amend the eighth paragraph in the BRIEF DESCRIPTION OF THE DRAWINGS section as follows:

Figs. 8A to 8E are cross-sectional views for explaining generation of bit lines of the data cell region of Fig. 1.

Please amend the paragraph beginning on line 14 of page 5 as follows:

Figs. 20A to 20C are cross-sectional views showing ~~generation~~ processes of generating word lines in the data cell substrate to be applied to a memory chip as the sixth embodiment of the present invention.

Please amend the paragraph beginning on line 19 of page 5 as follows:

Fig. 22 is a perspective view showing a ~~generation~~ process of generating word lines by means of the data cell substrate of Fig. 21.

Please amend the paragraph beginning on line 21 of page 5 as follows:

Fig. 23 is a perspective view showing a ~~generation~~ process of generating bit lines by means of the data cell substrate of Fig. 21.

Please amend the second full paragraph on page 6 as follows:

Fig. 26 is a perspective view showing a ~~generation~~ process of generating word lines by means of data cell substrate of Fig. 25.

Please amend the second full paragraph on page 6 as follows:

Fig. 27 is a perspective view showing a ~~generation~~ process of generating an insulation layer in the data cell substrate of Fig. 25.

Please amend the third paragraph on page 8 as follows:

The external connection electrode pad region 2D includes an external connection electrode pad connected to the system region 2A and each external connection electrode pad is connected, for example, to a terminal of a package by ~~the~~ a bonding method. The bit line electrode pad 2B connects the system region 2A and bit lines 5 of data cell region 3 and the word line electrode pad 2C connects the system region 2A and the word lines 4 of data cell region 3.

Please amend the second full paragraph on page 10 as follows:

Thereby, the desired data may be recorded or recorded data may be reproduced through the resistance values of the recording layer 7 which are different under the amorphous condition and crystallized condition. In other words, recorded data information may be represented by a set of resistance values within the recording layer 7, where these resistance values are a function of localized crystal structures within the recording layer 7. A known, predetermined voltage may be passed over one resistance value to generate a current I. ~~Current~~ The current I travels to sense amplifier 15 where it ~~current I~~ is detected and passed onto output circuit 17. Output circuit 17 employs binary discrimination to pass the recorded data information to the external connection electrode pads 2D.

Please amend the paragraph beginning on line 20 of page 12 as follows:

In this case, the layers up to the metal layer 4A may be removed by a single etching process ~~as required~~ or ~~the layers up to the metal layer 4A also may be removed by~~ a plurality of ~~times of~~ etching ~~process~~ processes. Here, an excellent result may be obtained by setting the etching rates of ultraviolet-setting resin 20, metal layer 4A, pn silicon layer 6A and recording film 7A to almost equal rate and then setting the etching rate of the memory substrate 2 to a very lower rate. In this case, selection ratio, stability and controllability of the etching

may be improved by introducing different kinds of material into the material of the metal layer 4A.

Please amend the paragraph beginning on line 23 of page 15 as follows:

Namely, the memory chip 1 may be formed by the following processes. After the metal layer 4A, pn silicon layer 6A and recording layer 7A are sequentially formed on the memory substrate 2, the ultraviolet-setting resin 20 is coated, and the protruded 70 and recessed 72 areas in the shape of word line 4 are formed by pressing the stamper 21 to this untraviolet-setting resin 20 (Fig. 5C). With the uniform etching utilizing this protruded 70 and recessed 72 areas, the metal layer 4A, pn silicon layer 6A and recording film 7A are removed conforming to the protruded 70 and recessed 72 areas. Thereby, the word line 4, and the pn silicon layer 6A and recording film 7A deposited on ~~this~~ the word line 4 may be formed.

Please amend the second full paragraph on page 17 as follows:

Accordingly, in the case of recording the desired data through change of resistance value due to change of the crystal structure of such recording layer 7, the so-called refresh operation by the charge accumulation mechanism in the DRAM of conventional devices ~~related art~~ may be omitted and the memory chip may be structured with ~~the as~~ a much simplified structure.

Please amend the first paragraph on page 18 as follows:

In more practical terms, since a data cell structure may be selected to record the desired data through change of resistance value due to the change of crystal structure of the recording layer 7, the memory of a more simplified structure may also be generated ~~also~~ with a more simplified process. In addition, since the structure of a data cell may be more simplified than conventional ~~the~~ semiconductor memory ~~of related art~~ by means of the charge accumulating mechanism, the large capacity memory also may be generated in ~~as~~ a much simplified structure.

Please amend the third full paragraph on page 20 as follows:

Next an insulating film 88 made of, for example, SiO_2 or Si_3N_4, ~~etc.~~ is formed in the data cell region 32 and thereby ~~insulation property~~ providing electrical insulation between the word lines ~~4 is assured.~~ As shown in Figs. 11A and 11B, after a liquid resin, for example, ~~of the~~ an ultraviolet-setting resin 36, is coated in the data cell region 32 (Figs. 11A and 11B), the resin is hardened to provide the flat surface thereof. Subsequently, the ultraviolet-setting region 36 is etched by ~~the~~ an etching method ~~which~~ that does not affect ~~give any influence on~~ the metal layer 4A and pn silicon layer 6A~~, for example,~~ such as, for example, ~~the~~ oxygen plasma etching~~, etc.~~ (Fig. 11C), and thereby the surface of the diode 6 which is protruded most from the memory substrate 31 may be exposed.